

<b>Notice of References Cited</b>	Application/Control No. 09/763,204	Applicant(s)/Patent Under Reexamination CLERMIDY ET AL.	
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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<del>B</del>	B	US-5,065,308	11-1991	Evans, Richard A.	714/11
<del>C</del>	C	US-6,681,316 B1	01-2004	Clermidy et al.	712/11
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
<del>U</del>	U	Chean et al. A Taxonomy of Reconfiguration Techniques for Fault-Tolerant Processor Arrays. IEEE Computer, pages 55-69.
<del>V</del>	V	Roychowdhury et al. Efficient Algorithms for Reconfiguration in VLSI/WSI Arrays. IEEE Transactions, vol. 39, no. 4. pages 480-489.
<del>W</del>	W	Belkhale et al. Reconfiguration Strategies for VLSI Processor Arrays and Trees Using a Modified Diogenes Approach. IEEE Transactions, vol. 41, no. 1. pages 83-96.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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